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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/897,574	07/02/2001	Kenichi Kawaguchi	10873.744US01	1221

7590 08/19/2004

Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/897,574	KAWAGUCHI, KENICHI	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Bauman et (US Patent 6,189,078)

As per claims 1, 6 Futral discloses a data transfer apparatus comprising:

- An associative memory (fig.5, 54) connected between a system bus (fig.5, 62) and a local bus(fig.5, 56); and
- A controller for controlling data input/output of the associative memory; (col.4, lines 12-19)
- Wherein the controller fetches an address and data that are transferred between devices on the system bus so as to duplicate and store them in the associative memory, accepts a data transfer request from the local bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the associative memory, reads out corresponding data from the associative memory so as to transfer it to the local/system bus. (col.5, lines 11-55)

As per claims 2, 7, Futral discloses wherein if it is detected that a write cycle of writing a data from one device to another device is generated on the system bus, the controller fetches the address and the data that are transferred between the devices so as to duplicate and store them in the associative memory. (col.5, lines 4-13)

As per claims 3,8, Futral discloses wherein the controller monitors a data output enable signal line of at lest one device controller on the system bus and, when the data output enable signal line is asserted, fetches the address and the data that are transferred on the system bus so as to duplicate and store them in the associative memory. (col.5, lines 36-55)

As per claims 4,9, Futral discloses wherein the controller monitors a data output strobe signal line of at least one device controller on the system bus and, when the data output strobe signal line is asserted, fetches the address and the data that are transferred on the system bus so as to duplicate and store them in the associative memory. (col.5, lines 14-55)

As per claims 5, 10, Futral discloses wherein when the address from which the data is transferred indicated by the data transfer request accepted from the local bus is not contained in the address stored in the associative memory, the controller stores a data effective information indicating the address in which a transfer operation has not been completed in response to the data transfer request in a second associative memory, fetches the address and the data that are transferred between the devices on the system bus and, if the fetched

address is the address indicated by the data effective information, transfers it to the local bus as data corresponding to the data transfer request. (col.4, line 41-col.5, line 13)

As per claim 11, Futral discloses a data transfer apparatus comprising:

- An associative memory (fig.5, 54) connected between a system bus(fig.5, 62) and a local bus(fig.5, 56); and
- A controller for controlling data input/output of the associative memory; (col.4, lines 12-19).
- Wherein the controller fetches an address and data that are transferred between devices on the system bus so as to duplicate and store them in the associative memory, fetches an address and a data that are transferred between devices on the local bus so as to duplicate and store them in the associative memory, accepts a data transfer request from the local bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the associative memory, reads out a corresponding data from the associative memory so as to transfer it to the local bus, accepts a data transfer request from the system bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the associative memory, reads out corresponding data from the associative memory so as to transfer it to the system bus. (col.5, lines 14-55)

As per claim 12, Futral discloses a data transfer method for controlling data input/output between a system bus and a local bus the method comprising:

A buffering operation of fetching an address and data that are transferred between devices on the system bus so as to duplicate and store them; and (col.4,lines 50-61), (col.3, lines 43-62)

An operation of accepting a data transfer request from the local bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the buffering operation, reading out corresponding data so as to transfer it to the local bus. (col.4, lines 41-61), (col.3, lines 43-62)

As per claim 13, Futral discloses a data transfer method for controlling data input/output between a system bus and a local bus, the method comprising:

- A buffering operation of fetching an address and data that are transferred between devices on the local bus so as to duplicate and store them; and (col.4, lines 41-61), (col.3, lines 43-62)
- An operation of accepting a data transfer request from the system bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the buffering operation, reading out corresponding data so as to transfer it to the system bus. (col.4, lines 41-61), (col.3, lines 43-62)

As per claim 14, Futral discloses a data transfer method for controlling data input/output between a system bus and a local bus, comprising:

- A first buffering operation of fetching an address and data that are transferred between devices on the system bus so as to duplicate and store them; (col.4, lines 41-61), (col.3, lines 43-62)
- A second buffering operation of fetching an address and data that are transferred between devices on the local bus so as to duplicate and store them; (col.4, lines 41-61), (col.3, lines 43-62)
- A first data transfer operation of accepting a data transfer request from the local bus and, when address from which the data is transferred indicated by the data transfer request is contained in the address stored in the first buffering operation, reading out corresponding data so as to transfer it to the local bus; and (col.4, lines 41-61)
- A second data transfer operation of accepting a data transfer request from the system bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the second buffering operation, reading out corresponding data so as to transfer it to the system bus. (col.4, lines 41-61)

Response to Amendment

3. Applicant's amendment filed on 5/5/04 have been fully considered but are moot in view of the new ground(s) of rejection.

a. In response to applicant's argument that Bauman does not teach or suggest that data is transferred between devices on the system bus. However, as Futral notes at col.3, lines 45-62, discloses DMA accesses data stored in a memory 38, operating as programmed by destination i/o adapter. Once the data is accessed, it is transferred to the destination i/o adapter. The memory controller received commands and data and transmits data over primary bus.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

August 12, 2004

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100